CLAIM LISTING

This listing of claims will replace all prior versions and listings of claims in the application:

IN THE CLAIMS

Please cancel Claim 2 without prejudice.

1. (Currently Amended) A JTAG-compliant chip for communicating with a non-JTAG-compliant chip comprising:

a JTAG-compliant test access port (TAP) controller integrated on a programmable logic device (PLD);

a TAP input pin coupled to the TAP controller on the PLD;

a boundary scan shift register coupled to the TAP input pin and to the TAP controller;

a plurality of pins of the PLD coupled to the first shift register and coupled ~~extending from the JTAG-compliant chip~~ to the non-JTAG-compliant chip; and

a controller implemented on programmable logic resources of the PLD coupled ~~connected~~ to:

receive signals from a second shift register that is coupled to the TAP input pin and implemented on programmable logic resources of the PLD, and

in response to the signals from the shift register and the TAP controller, send and receive signals on the plurality of PLD pins coupled ~~extending from the JTAG-compliant chip~~ to the non-JTAG-compliant chip.

2. (Cancelled)

3. (Original) The JTAG-compliant chip of Claim 1 wherein the TAP controller accesses external TDI and TDO control signals.

4. (Original) The JTAG-compliant chip of Claim 3 wherein the TAP controller allows the controller to access the external TDI and TDO control signals.

5. (Currently Amended) The JTAG-compliant chip of Claim 1 wherein the controller comprises~~:~~

~~a shift register connected to external TDI and TDO control signals; and~~

a state machine that in response to commands in the shift register sends and receives signals on the plurality of PLD pins ~~extending from the JTAG compliant chip to the non JTAG compliant chip~~.

6. (Currently Amended) The JTAG-compliant chip of Claim 1 wherein the controller uses the signals on the plurality of PLD pins ~~extending from the JTAG compliant chip to the non JTAG compliant chip~~ to write to and read from the non-JTAG-compliant chip.

7. (Currently Amended) The JTAG-compliant chip of Claim 6 wherein the non-JTAG-compliant chip is a flash memory chip and the controller further uses the signals on the plurality of PLD pins ~~extending from the JTAG compliant chip to the non JTAG compliant chip~~ to erase the flash memory chip.

8. (Currently Amended) The JTAG-compliant chip of Claim 1 ~~2~~ wherein the programmable logic device is a field programmable gate array chip.

9. (Currently Amended) A method of using a programmable logic device ~~chip~~ having a boundary scan structure to access a chip not having a boundary scan structure comprising:

programming the programmable logic device ~~chip~~ having the boundary scan structure to implement a shift register and a controller for:

receiving boundary scan input signals,

providing boundary scan output signals,

providing signals to the chip not having a boundary scan structure, and

receiving signals from the chip not having a boundary scan structure.

10. (Original) The method of Claim 9 wherein the step of providing signals to the chip not having a boundary scan structure comprises providing commands to indicate one of a plurality of operations to be performed.

11. (Original) The method of Claim 10 wherein the step of providing signals to the chip not having a boundary scan structure further comprises providing an address to the chip not having a boundary scan structure.

12. (Original) The method of Claim 11 wherein the step of providing signals to the chip not having a boundary scan structure further comprises providing data to the chip not having a boundary scan structure.

13. (Original) The method of Claim 9 wherein the step of receiving signals from the chip not having a boundary scan structure comprises receiving data from the chip not having a boundary scan structure addressed by some of the signals provided in the step of providing signals to the chip not having a boundary scan structure.

14. (Currently Amended) A method of configuring a non-JTAG chip from a JTAG-compliant programmable logic device (PLD) ~~chip~~ having programmable logic resources ~~core logic~~, the method comprising the steps of:

a. loading an instruction into a JTAG TAP interface of the PLD ~~JTAG compliant chip~~ that causes the JTAG TAP interface to enable a path for serial data transfer ~~to go~~ from a JTAG-compliant TDI pin to the ~~core~~ programmable logic resources of the PLD ~~JTAG compliant chip~~;

b. defining a shift register in the ~~core~~ programmable logic resources of the PLD ~~JTAG compliant chip~~ that receives data transferred from the TDI pin; and

c. defining a controller in programmable logic resources of the PLD that receives the shift register data in parallel with the JTAG TAP interface and generates from this data signals applied to pins of the PLD ~~JTAG-compliant chip~~ that are coupled ~~connected~~ to pins of the non-JTAG chip.

15. (Currently Amended) The method of Claim 14 wherein the shift register defined in the programmable ~~core~~ logic resources of the JTAG-compliant chip outputs data to a JTAG-compliant TDO pin.

16. (Original) The method of Claim 14 comprising the additional step performed by the controller of receiving signals from the non-JTAG chip.

17. (Original) The method of Claim 14 wherein the shift register comprises two shift registers, one of which receives address data for addressing part of the non-JTAG chip and another of which receives data words for being loaded into the non-JTAG chip.

18. (Original) The method of Claim 14 wherein the shift register receives both address data for addressing part of the non-JTAG chip and data words for being loaded into the non-JTAG chip.

19. (Original) The method of Claim 18 wherein the address data is loaded into the shift register first, and becomes a starting address for subsequent data words to be loaded into the non-JTAG chip, and is incremented internally by the controller for loading a plurality of the data words.

20. (Original) The method of Claim 18 wherein the address data, data word, and any other data needed by the non-JTAG chip are applied in parallel to the non-JTAG chip.

21. (Original) The method of Claim 20 wherein the address data, data word, and any other data needed by the non-JTAG chip configure part of the non-JTAG chip.

22. (New) A programmable logic device (PLD), comprising:

a plurality of programmable logic, input/output, and routing resources;

a plurality of input/output pins coupled to the plurality of programmable input/output resources;

a test data input (TDI) pin;

a scan register coupled to the TDI pin;

an instruction register coupled to the TDI pin;

a boundary scan controller coupled to the TDI pin, the scan register, and the instruction register, the boundary scan controller adapted to activate a first signal in response to a first instruction code in the instruction register;

a shift register implemented in programmable logic resources of the PLD, coupled to the TDI pin, and coupled to a subset of the input/output pins; and

a control circuit implemented in programmable logic resources of the PLD and coupled to the shift register and to the subset of input/output pins, the control circuit adapted to enable shifting of data from the TDI pin to the shift register responsive to activation of the first signal, and perform one of a read operation and a write operation on the subset of input/output pins responsive to a state of at least one of the bits in the shift register.

23. (New) The PLD of claim 22, wherein the control circuit is further adapted to read data from the subset of input/output pins and store the data in the shift register responsive to a first state of the at least one control bit in the shift register.

24. (New) The PLD of claim 23, wherein the control circuit is further adapted to write data from the shift register to the subset of input/output pins responsive to a second state of the at least one control bit in the shift register.

25. (New) The PLD of claim 24, wherein the instruction code is a code reserved for signaling a non-boundary-scan circuit from a boundary scan controller.

26. (New) The PLD of claim 24, wherein the at least one control bit in the shift register includes at least two control bits, and the control circuit is further adapted to generate signals at the subset of input/output pins for erasing data on a memory chip coupled to the PLD in response to a third state of the at least two control bits.

27. (New) The PLD of claim 26, wherein the control circuit is further adapted to generate signals at the subset of input/output pins for erasing data from a subset of addressable memory on the memory chip in response to a fourth state of the at least two control bits.

28. (New) A method for accessing a non-boundary scannable memory via a programmable logic device (PLD), comprising:

implementing a control circuit and a shift register coupled to the control circuit on programmable logic, input/output, and routing resources of the PLD;

coupling the shift register to a test data input (TDI) pin of the PLD, and coupling the control circuit to a boundary scan controller of the PLD with programmable routing resources of the PLD;

coupling the shift register to a subset of input/output pins of the PLD with routing resources of the PLD;

activating a first signal by the boundary scan controller in response to a first instruction code in a boundary scan instruction code register;

enabling shifting of data from the TDI pin to the shift register by the control circuit in response to the activated first signal; and

generating access signals at the subset of input/output pins by the control circuit in response to a state of at least one control bit in the shift register.

29. (New) The method of claim 28, further comprising reading data at the subset of input/output pins and storing the data in the shift register by the control circuit in response to a first state of the at least one control bit in the shift register.

30. (New) The method of claim 29, further comprising writing data from the shift register to the subset of input/output pins by the control circuit in response to a second state of the at least one control bit in the shift register.

31. (New) The method of claim 30, wherein the at least one control bit in the shift register includes at least two control bits, the method further comprising generating signals at the subset of input/output pins for erasing data on a memory chip coupled to the PLD by the control circuit in response to a third state of the at least two control bits.

32. (New) The method of claim 31, further comprising generating signals at the subset of input/output pins for erasing a subset addressable memory of the memory chip by the control circuit in response to a fourth state of the at least two control bits.

33. (New) The method of claim 28, wherein the instruction code is a code reserved for signaling a non-boundary-scan circuit from a boundary scan controller.